ebalanceplus

D3.4 - Specification and implementation of grid automation and control devices and interfaces

Deliverable D3.4

Date: 31/01/2022

Author(s): Sami Hammal (EMT)

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Technical References

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[1] PU = Public

PP = Restricted to other programme participants (including the Commission Services)

RE = Restricted to a group specified by the consortium (including the Commission Services)

CO = Confidential, only for members of the consortium (including the Commission Services)

Document history

V	Date	Beneficiary(ies)	Author(s)
1	31-Jan-2022	EMTECH	Sami Hammal
2			
3.1			

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Summary

Part of the ebalance-plus platform is to design and develop a set of control and automation units, called Grid Management Units, to be installed at MV/LV level and in DER locations. This deliverable describes the need to have these automation units and their structure regarding architecture and operation. In detail:

Section 1 – Introduction, provides a brief introduction about the deliverable position w.r.t. its work package and other related work packages, and a list of reference documents

Section 2 – High-level System Architecture, provides a high-level system architecture description of the grid management units

Section 3 – Management Units, provides more details regarding the inner structure of each grid management unit in terms of modules, interfaces, and specifications.

Section 4 – Conclusion, provides a final conclusion about the deliverable and the grid management unit in the context of the ebalance-plus project

Disclaimer

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Abbreviations and Acronyms

AC	Alternating Current
ACQ	Acquisition
ADC	Analogue-to-Digital Converter
AFE	Analogue Front-End
AIN	Analogue Input
AOUT	Analogue Output
BoM	Bill of Materials
CMU	Customer Management Unit
CO2	Carbon Dioxide
DAQC	Data Acquisition and Control
DC	Direct Current
DER	Distributed Energy Resources
DERMU	Distributed Energy Resources Management Unit
DIN	Digital Input
DMA	Direct Memory Access
DOUT	Digital Output
DSO	Distribution System Operator
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMIF	External Memory Interface
EMT	EMTECH SPACE P.C.
ETH	Ethernet
FW	Firmware
GND	Ground
GPIO	General Purpose Input/output
GPS	Global Positioning System
GW	Gateway
I2C	Inter-Integrated Circuit
IEC	International Electrotechnical Commission
IF	Interface
I/O	Input/output

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ISP	In-System Programming
LCD	Liquid-Crystal Display
LV	Low-Voltage
LVGMU	Low Voltage Grid Management Unit
MCU	Microcontroller
MMC	Multimedia Card
MV	Medium-Voltage
MVGMU	Medium Voltage Grid Management Unit
PCB	Printed Circuit Board
PI	Power Inverter
PMU	Phasor Measurement Unit
PPS	Pulse per second
PV	Photovoltaic
RAM	Random Access Memory
SD	Secure Digital
SoC	System on Chip
SPI	Serial Peripheral Interface
SW	Software
TFT	Thin-Film Transistor
TSO	Transmission System Operator
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
USB	Universal Serial Bus
V2G	Vehicle to Grid
w.r.t.	With respect to

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1 Introduction

1.1 Deliverable Position

Figure 1 below shows the position of this deliverable within the context of the ebalance-plus project. The current deliverable is part of work package WP3 – Solutions Grid Flexibility Resilience and it is the output of task T3.4 - Automation and control solutions for grid resilience. This deliverable is input to the deliverable D4.2 – Report on Algorithms at MV/LV level [RD-1], part of work package WP4 – Energy Balancing Platform, and to work package WP6 – Demonstration and Evaluation.

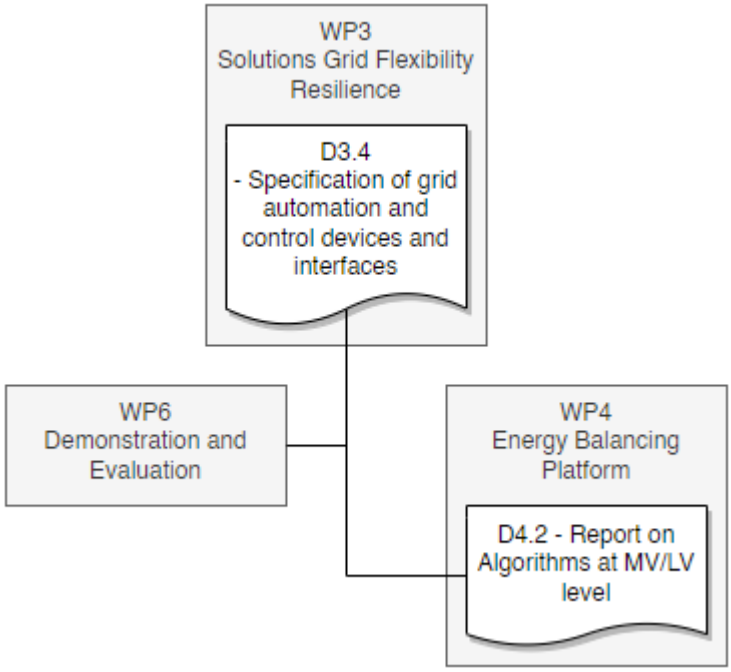

Figure 1: D3.4 Deliverable position

1.2 Reference Documents

Ref.	Title
[RD-1]	D4.2 - Report on Algorithms at MV_LV level
[RD-2]	Texas Instruments C5000 Ultra-low power DSP http://www.ti.com/processors/digital-signal-processors/c5000-low-power-dsp/overview.html *last visited: 20-Jan-2022*
[RD-3]	Texas Instruments http://www.ti.com/ *last visited: 20-Jan-2022*

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[RD-4]	TRACO Power *https://www.tracopower.com/home/* *last visited: 20-Jan-2022*
[RD-5]	Microchip *https://www.microchip.com/* *last visited: 20-Jan-2022*
[RD-6]	XMODEM *https://en.wikipedia.org/wiki/XMODEM* *last visited: 20-Jan-2022*

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2 High-level System Architecture

2.1 Grid-level System Architecture

This section provides a general description of the ebalance-plus project with respect to the Management Units explaining their need and their position on a grid-level.

The aim of the ebalance-plus project is to create an energy-balancing platform to provide the appropriate flexibility of energy grids and increase their resilience. This platform aims to minimise the energy costs, reduce the CO2 emissions and increase energy efficiency. To support this energy balancing platform, different devices, equipment and other hardware/software solutions are developed and enhanced within the context of the ebalance-plus project from different members of the consortium. The content of the current document provides a description regarding a set of management units to be installed in key locations of the grid to perform the required demonstration and evaluation of the platform.

The ebalance-plus concept consists of (1) increasing/unlocking the energy flexibility by means of smart-grid solutions, (2) predicting the available flexibility (in buildings, DER, EVs and distribution grids), (3) managing the grid flexibility by means of new business models and resilience services with the energy aggregator as facilitator, (4) developing smart-grid solutions to increase the LV and MV grid monitoring and automation levels to avoid critical risks (power peaks, congestions, etc.) and (5) engaging end-users in project developments (e.g. graphical user interface) to guarantee the acceptance of demonstrated solutions. Figure 2 below illustrates the ebalance-plus environment and its five main elements stated above. As depicted, the different types of management units that monitor and control the different fields and components of the ebalance-plus concept are shown: customer management unit (CMU), Distributed Energy Resources management units (DERMU), low voltage grid management unit (LVGMU) and medium voltage grid management unit (MVGMU). CMU and DERMU send the status of buildings and DER units to the LVGMU, which is monitored by DSOs and the energy aggregator. Then, the energy aggregator through the LVGMU collects and calculates the available flexibility with the developed prediction models. In turn, the DSO receives the available flexibility and, according to the grid status provided by the smart-grid solutions, decisions are made (with the support of an automatic advisor) about the amount of flexibility that must be released to keep the system under secure and stable conditions. On the other hand, the MVGMU provides optimum voltage and reactive power regulation at MV level and facilitates flexibility at TSO-DSO level. At the building level, ebalance-plus provides IoT and smart-storage systems to increase the building and facility flexibility. At grid level, the V2G and power inverter (PI) technologies are provided to create high-efficient DC networks and power-to-X technologies controlled by the DERMU. Figure 2 represents in different colours the systems provided by ebalance-plus and the existing ones in the project pilots. In addition, smart-grid solutions are provided to increase the grid observability and allow DSOs to make better decisions on energy flexibility as an important value for grid resilience.

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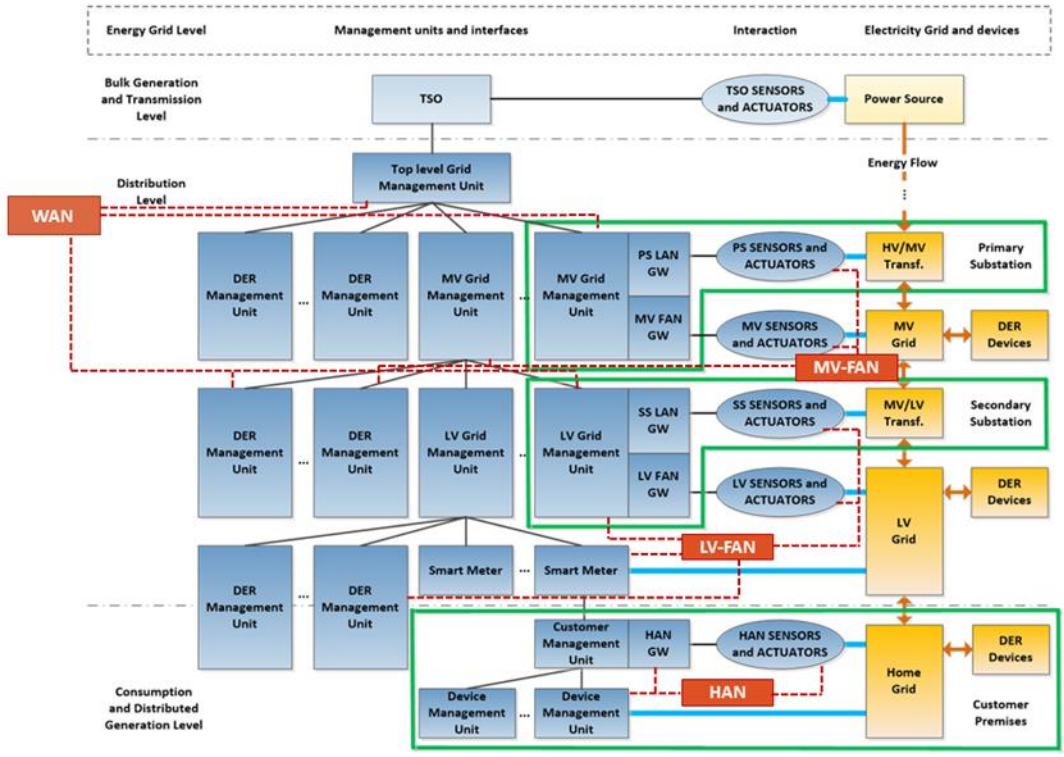

Figure 2: ebalance-plus concept, system architecture and flexible solutions in smart grids

All grid management units (GMU) provide the ability to acquire measurements (data), store them locally (in case of communication loss), communicate with the energy balancing platform to provide the measurements, receive commands from the platform to control assets or give local commands if the intelligence is processed at the network edge. The data to be stored are quantities measured in electrical systems - such as voltage, current, power, frequency etc. Rate of data collection is adapted according to specific needs (geographical scales and grid level).

2.2 Grid Management Units Architecture

This section provides a description regarding the architecture of the Management Units showing their top-level elements & common modules, techniques used in the development on both hardware and firmware level. Each of the following sub-sections describes the top-level architecture of that particular device specifying its main components and functionalities.

Essentially, the management units are the low-level devices that enables the actuation between the algorithms and the corresponding equipment, sensors, actuators, and devices that need to be controlled and read data from using the appropriate interfaces that are commonly used in power grid management applications. In summary, the three MUs are presented below:

MVGMU: Medium Voltage Grid Management Unit, this device is installed in high to medium voltage primary distribution substations and its main function is to monitor the substation transformer, measure the grid voltage & current, the active power (MW), reactive power (MVAr) and voltage (kV) as core parameters, and to automate the reactive power compensation in power distribution substations. Depending on the

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available infrastructure – through availability of input signals – the MVGMU device provides the ability to monitor additional assets, such as the On-Line Tap Changer (OLTC), the capacitor banks or any other voltage regulation and reactive power compensation assets used to maintain the desired voltage levels. Therefore, the MVGMU with the ebalance-plus platform will be able to suggest (decision support) or automatically control the assets under optimised operation schemes (e.g., joint Volt/VAr control).

LVGMU: Low Voltage Grid Management Unit, this device is installed in secondary distribution substations to monitor the transformer, the power quality and faults, and its function is to continuously measure the voltage and the current of the grid to provide a set of measurements to the higher level, where decisions are taken based on adjustable criteria. This unit provides information about the distribution grid quality parameters (power flows, voltage level, etc.) using also the information from DERMU and other smart-grid technologies installed in the LV grid and secondary substation. This unit also contains district prediction models to provide the available flexibility 24-hours in advance with a resolution of 15 minutes. The energy aggregators are responsible for accounting the energy flexibility released, supporting DSO and managing the steering signals. Additionally, the LVGMU supports the synchronization of measurements between different management units using GPS to provide the ability for further analysis and to easily correlate the occurrences of specific chain of events.

DERMU: Distributed Energy Resources Management Unit, this is a compact device that supports edge computing, like all other MUs, and it's installed in DER assets to communicate with ebalance-plus and give commands to the assets where the management of energy resources is crucial for the operation of the grid. Moreover, DERMU provides the ability to the facility managers and DER managers to exploit their assets. The principle of operation of the ebalance-plus solution is to continuously find optimized power-flow grid conditions and to apply the results to DER assets via the DERMU, to set the optimal points of operation. The device includes a set of commonly used interfaces to support a wide selection of external devices and equipment to be connected (Diesel generators, Inverters etc.)

2.2.1 MVGMU

Figure 3 below depicts the top-level logical structure of the MVGMU device. As shown, the key modules are the ones listed below:

- Gateway (GW)
- Phasor Measurement Unit (PMU)
- Data Acquisition and Control (DAQC)
  - MCU
  - Digital Input (DIN)
  - Digital Output (DOUT)
  - Analogue Input (AIN)
  - Analogue Output (AOUT)
  - Display
  - Keypad
- Power supply unit

Each of the elements above are described in detail in the following sub-sections. The display and the keypad is part of the User Interface, which is used to provide

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information regarding the state of the device, measurements, operation, grid status etc. and to configure the device on-site. The Data Acquisition and Control includes a set of digital and analogue input/output interfaces commonly used in industrial and power distribution substations environments. These are provided to offer the option to control external actuators/equipment, and to read from external devices/sensors compatible with the same interface. The Phasor Measurement Unit is used to acquire high sampling voltage and current measurements from the substation transformer. The Gateway is essentially the network interface between the device and the local network where the management unit is installed. Moreover, the GW is where the grid resilience algorithms reside and are executed. Finally, the power supply unit includes all the necessary components required to provide power to the device from the 230VAC input.

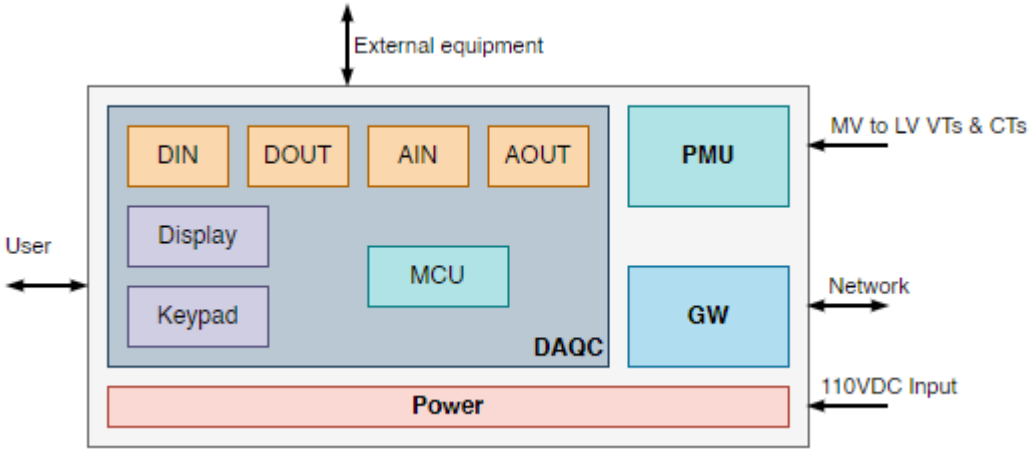

Figure 3: MVGMU top-level logical diagram

2.2.2 LVGMU

Figure 4 below depicts the top-level logical diagram of the LVGMU device showing its key modules, which are:

- Gateway (GW)
- Phasor Measurements Unit (PMU)
- Power supply unit

There are many similarities between each management unit regarding their utilized modules. Specifically, the LVGMU includes the PMU and the GW modules to acquire voltage and current measurements from the transformer and to provide an Ethernet interface for the device to be connected to the local network. Additionally, just like in the MVGMU device, the power supply follows the same design principle, where the 230VAC input is converted to a compatible DC voltage to provide the appropriate power to the device.

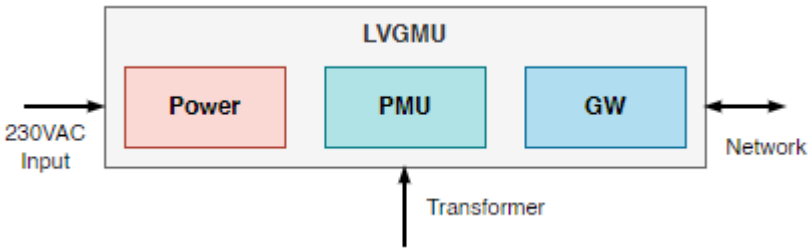

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Figure 4: LVGMU top-level logical diagram

2.2.3 DERMU

Figure 5 below depicts the top-level logical structure of the DERMU device showing its key modules in the list below:

- Gateway (GW)
- Data Acquisition and Control (DAQC)
  - MCU
  - Digital Input (DIN)
  - Digital Output (DOUT)
  - Analogue Input (AIN)
  - Analogue Output (AOUT)
- Power supply unit

As with the other management units, the DERMU includes the Gateway module to provide the required connectivity to the local network and to execute the grid resilience algorithms. Additionally, the DERMU includes a set of digital and analogue input/output interfaces to provide a seamless connection to external devices, sensors, equipment, and other commonly used Distributed Energy Resources units (Diesel generators, photovoltaic parks, wind farms, weather stations etc.)

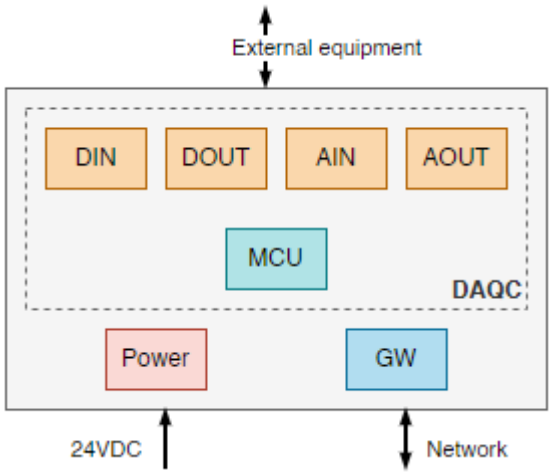

Figure 5: DERMU top-level logical diagram

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3 Management Units

The following sections will provide a detailed description regarding each management unit. Due to the similarities between these devices, the sub-sections of each section regarding each device are kept the same and only the differences are provided in each of the following, thus section 3.1 includes the full description regarding all modules, and the following sub-sections in sections 3.2 & 3.3 include references to those unless there are major differences in structure of the modules of that particular device, which are additionally described.

The text below mainly focuses on the structure of the modules used in each management unit on a logical level, meaning that the physical structure is different for each MU, but the logical structure remains the same. Due to the differences in the mechanical arrangement between each management unit, the physical structure (electronic circuit placement and PCB design) is designed to accommodate the enclosure of the corresponding management unit. Information about the mechanical aspects of each device is provided in a separate sub-section, where the physical structure is described.

3.1 MVGMU

3.1.1 Gateway

This sub-section describes the gateway (GW) module regarding its inner components & their internal interfaces and its external interfaces with other modules. Main component of the GW is the OSD3358 System-on-Chip (SoC), which is capable of running a Linux operating system required to execute the main software. Some of the key-features of the OSD3358 SoC are:

- Based on the TI [RD-3] Sitara™ AM335x ARM® Cortex® A8 Processor
- Up to 1 GHz
- Ethernet 10/100/1000
- MMC, SD, and SDIO
- Up to 1 GB DDR3L memory
- CAN, SPI, I2C, UART, GPIO etc.

Figure 6 below shows the logical structure of the GW module. As depicted, the OSD3358 provides the following interfaces:

- MMC: to interface with the SD memory card storing the OS and all the data
- I2C: to interface with the on-board EEPROM memory
- UART: to interface with the PMU and other external modules
- Ethernet: to provide an Ethernet interface to connect to the local network

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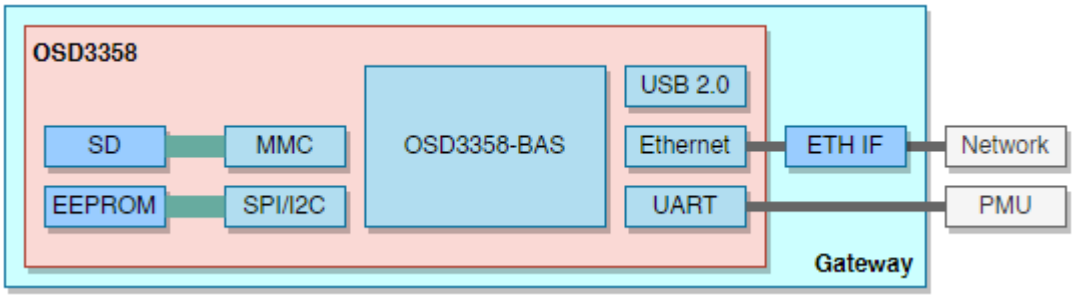

Figure 6: Gateway structure

As shown is Figure 6, the OSD3358 board is segregated from the gateway module, it is essentially a separate board that is connected to the gateway module. This board includes the most essential elements to make the OSD3358 SoC operate properly, and all the interfaces are exposed to two mezzanine connectors to be used in other designs depending on the application. This is done to simplify the design process and to easily accommodate different designs utilized in different devices.

Figure 7 below depicts the top side of the OSD3358 board regarding its key component, which is the OSD3358 SoC, and part of the gateway module. The logical structure of the gateway modules remains the same in all of the management units, however, depending on the MU, the physical structure is adapted accordingly to accommodate the respective device mechanical constraints. Figure 8 below depicts the bottom side of the same OSD3358 board showing the mezzanine connectors to provide a picture on how the board is mounted onto the gateway board.

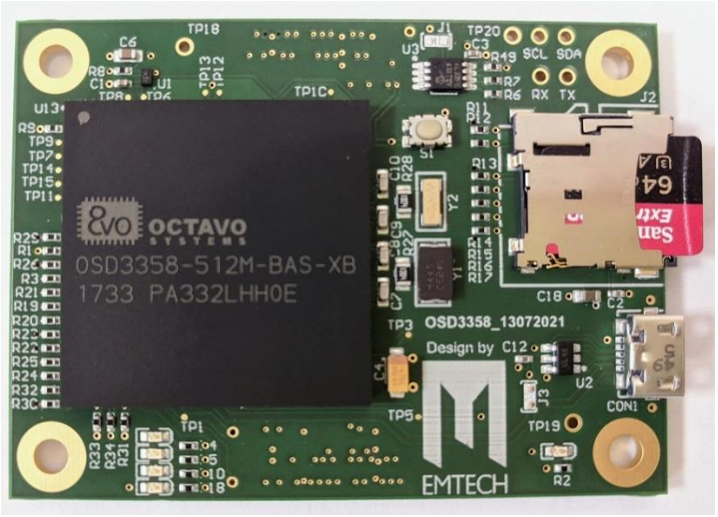

Figure 7: OSD3358 board (top side)

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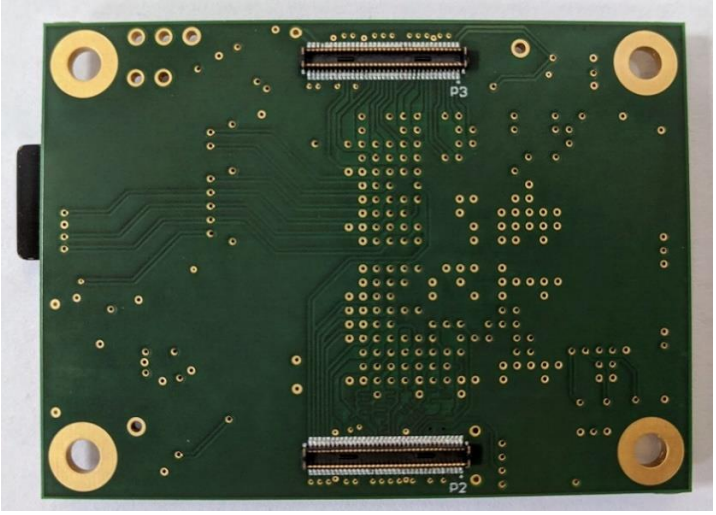

Figure 8: OSD3358 board (bottom side)

The gateway module plays a significant role in all management units, because it provides the interfaces and mechanisms required to support edge computing and run the grid resilience algorithms. For more details about the grid resilience algorithms refer to D4.2 – Report on algorithms to increase grid resilience at LV/MV level [RD-1].

Essentially, the GW constitutes the network interface between the device and other external equipment, devices, actuators, and sensors. It is included in all management units to provide the means needed to connect to the local network where the device is installed.

3.1.2 User Interface

The user interface of the MVGMU includes a display and a keypad. The display is a 5.0” TFT colour LCD as shown in Figure 9 below. The keypad is a 16-key membrane keypad as shown in Figure 10 below.

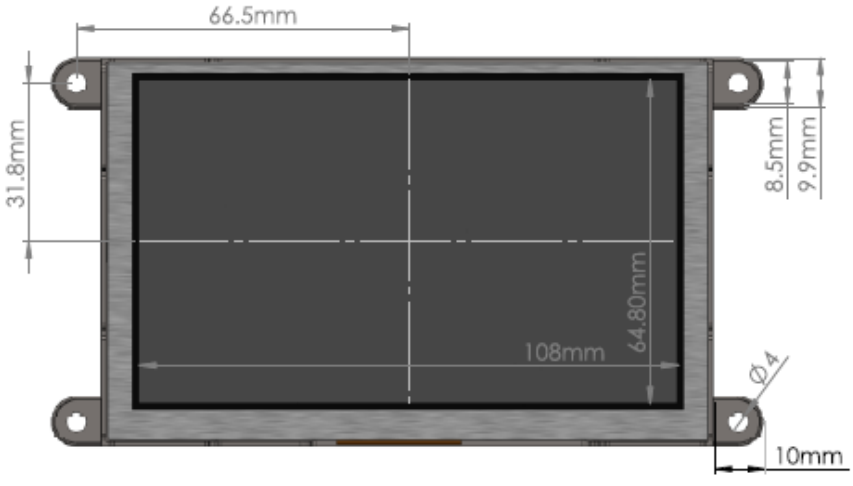

Figure 9: MVGMU display module

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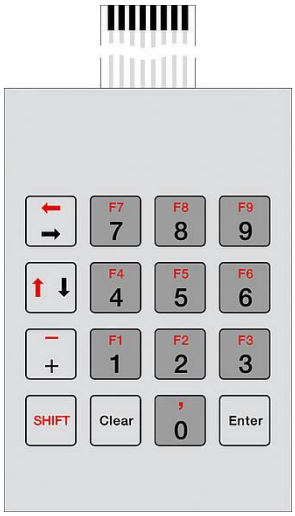

Figure 10: MVGMU keypad

The user interface is used to show the status of the device and to provide the means to configure the device on-site. A simple navigation menu is provided to configure the device and a home page showing the most basic measurements.

3.1.3 Data Acquisition and Control

This section describes the data acquisition and control module of the MVGMU device showing its main elements and interfaces. The data acquisition and control includes a set of analogue and digital inputs and outputs to provide the appropriate interfaces to acquire and control external devices and equipment commonly found in primary distribution substations. In the following text, a logical description is provided for each interface, and finally, an overall description on how all these interfaces are bonded together in the context of the MVGMU device.

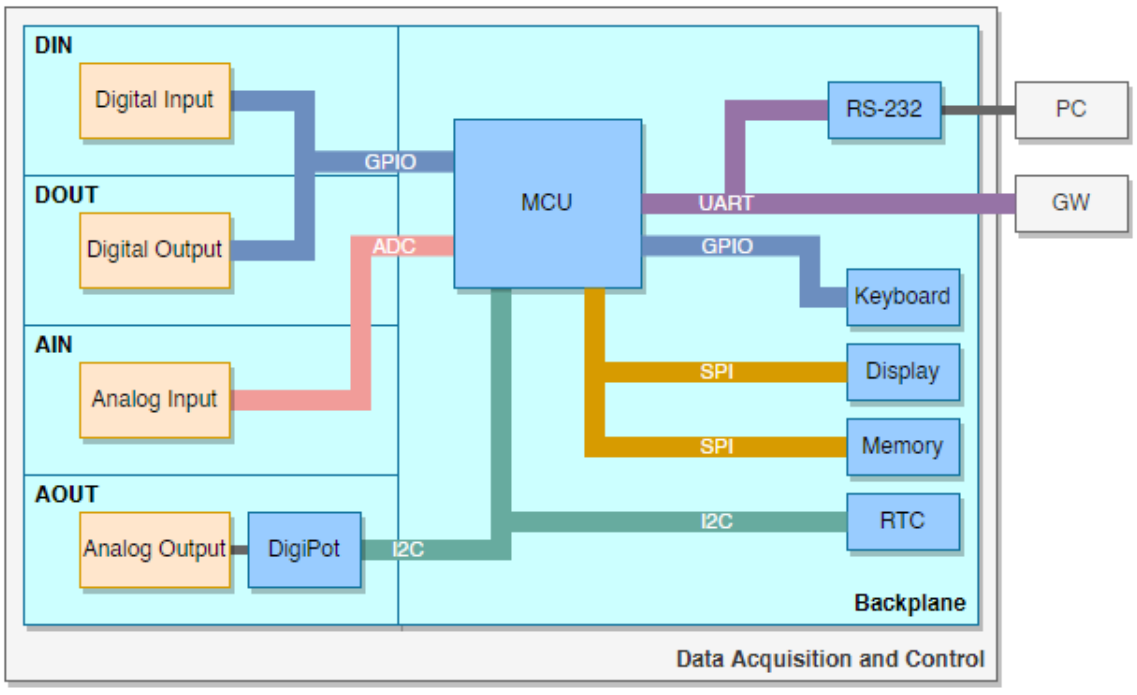

Figure 11: Data acquisition and control logical structure

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Figure 11 above shows the logical structure of the data acquisition and control module. As depicted, the main component is the microcontroller (MCU) that handles the communication between the DAQC module and the GW, the control of the digital and analogue interfaces, and the control of the display and the keyboard. Each individual interface type is described in the subsections below. In addition, the DAQC module includes an RTC chip to keep the time and to add time stamps to the acquired measurements. A non-volatile memory is also utilized to store some basic parameters regarding operation, and calibration coefficients. Moreover, the control of the display and the reading of the keyboard is handled here by the MCU. The interface of the display is SPI and the keyboard is based on simple GPIO lines coded to map its 16 pads. There are differences between the logical and the physical structure of the DAQC module, and Figure 11 above depicts mainly the logical structure with some hints about the physical. The section labelled as “Backplane” includes all the digital circuitry of the DAQC, and this part physically resides in its own board. Each of the remaining sections regarding each interface also reside physically in their own individual board. Each interface board is connected vertically with the backplane board using mezzanine board-to-board connectors. Some of the specifications regarding the MCU are:

- 8-bit AVR series from Microchip [RD-5]
- Up to 24 MHz clock
- 128 KB Flash, 16 KB RAM, 512 B EEPROM
- Peripherals: UART, SPI, I2C, 12-bit ADC, 10-bit DAC, AC, 16-bit Timers, GPIO
- 64-pin package

Figure 12 below depicts a 3D picture of the Backplane PCB showing its components including the MCU and the mezzanine connectors where the other PCBs are mounted vertically.

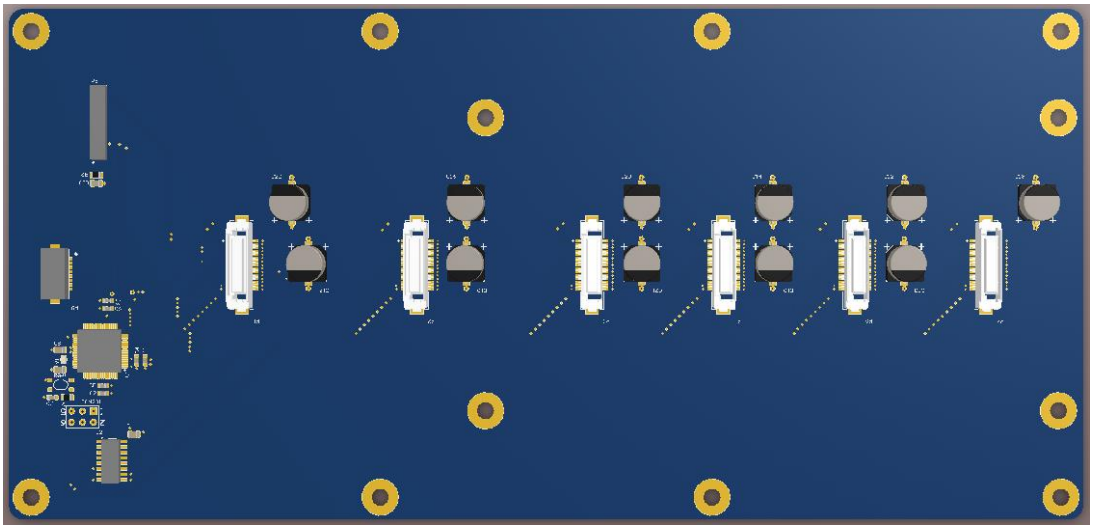

Figure 12: DAQC – Backplane PCB

3.1.3.1 Digital input

Figure 13 below depicts the logical structure of the digital input (DIN) interface. As shown, the digital input interface is consisted of a simple voltage divider to reduce the input to a level acceptable by the optocoupler, which provides the appropriate isolation needed between the input and the main digital circuitry, and to translate the input

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voltage to a binary 1 or 0, which is acquired by the microcontroller interfaced with it. The isolation is an important feature that is provided in all the interfaces presented (DIN, DOUT, AIN, AOUT) and its main function is to isolate the input from the internal part of the device and to offer a high protection from any external triggers that might occur, if the input is connected to outside equipment. Some of the optocoupler's specifications are:

- High speed: 1 Mb/s
- TTL compatible
- Open collector output
- Insulation: 3750 Vrms for 1 minute

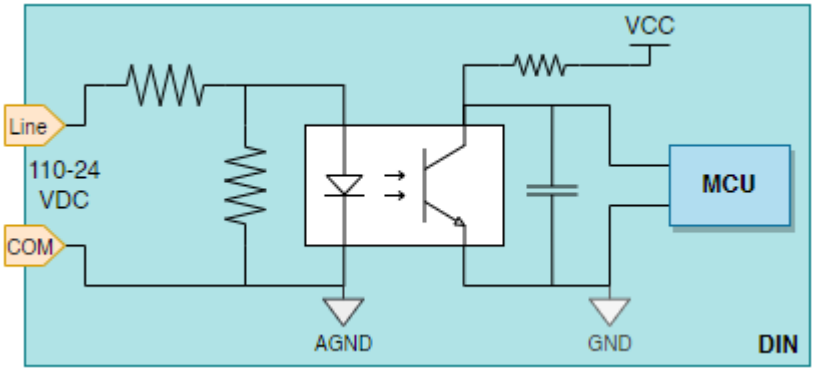

Figure 13: Digital Input logical structure

Figure 14 below depicts a 3D picture of the digital input interface PCB showing its components. On the left (white colour) the mezzanine connector is placed that connects this board to the backplane board, and on the right, the large (blue colour) connector is the interface connector with the external environment.

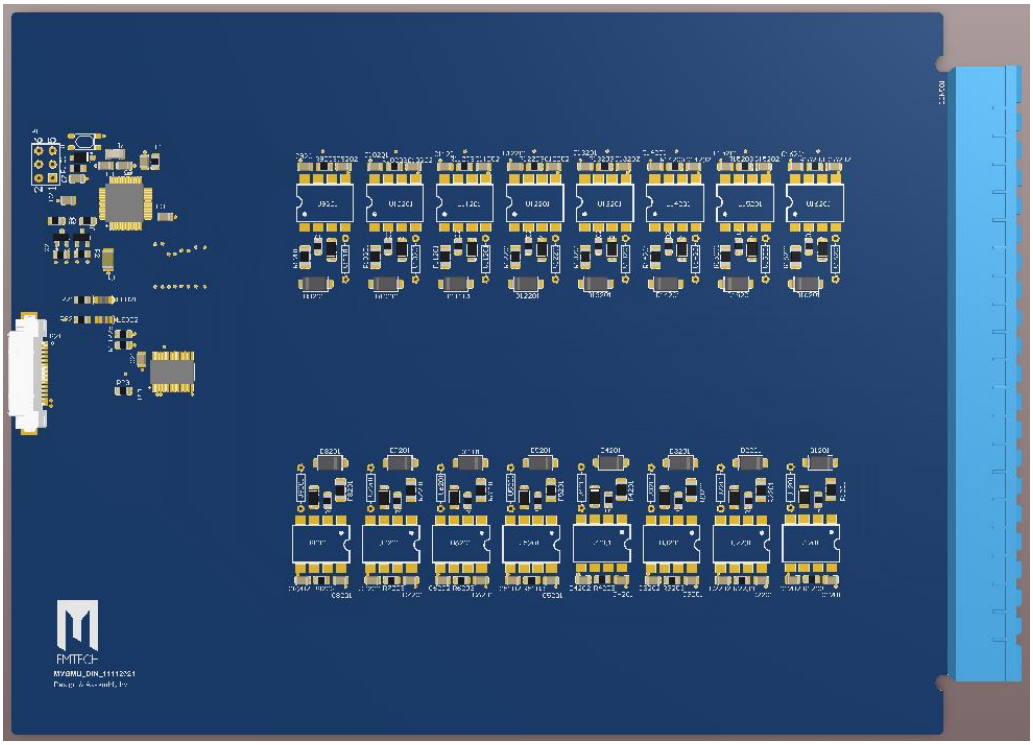

Figure 14: Digital Input PCB

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3.1.3.2 Digital Output

Figure 15 below shows the logical structure of the digital output (DOUT) interface. As depicted, the digital output is nothing more than a power relay controlled by the microcontroller that is utilized using a transistor for engaging and disengaging the relay. DOUT provides two pins, Line & COM, that are connected to the external device or equipment to be controlled by the device. Some of the relay's specifications are listed below:

- Rated Voltage: 250VAC
- Rated Current: 8A
- Contact arrangement: DPDT, 2 from C (CO) or 2 from A (NO)
- Insulation: 5000Vrms (between contact and coil)

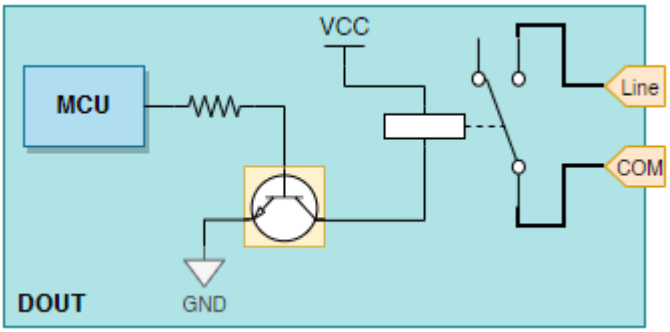

Figure 15: Digital output logical structure

Figure 16 below depicts a 3D picture of the DOUT interface PCB showing its components.

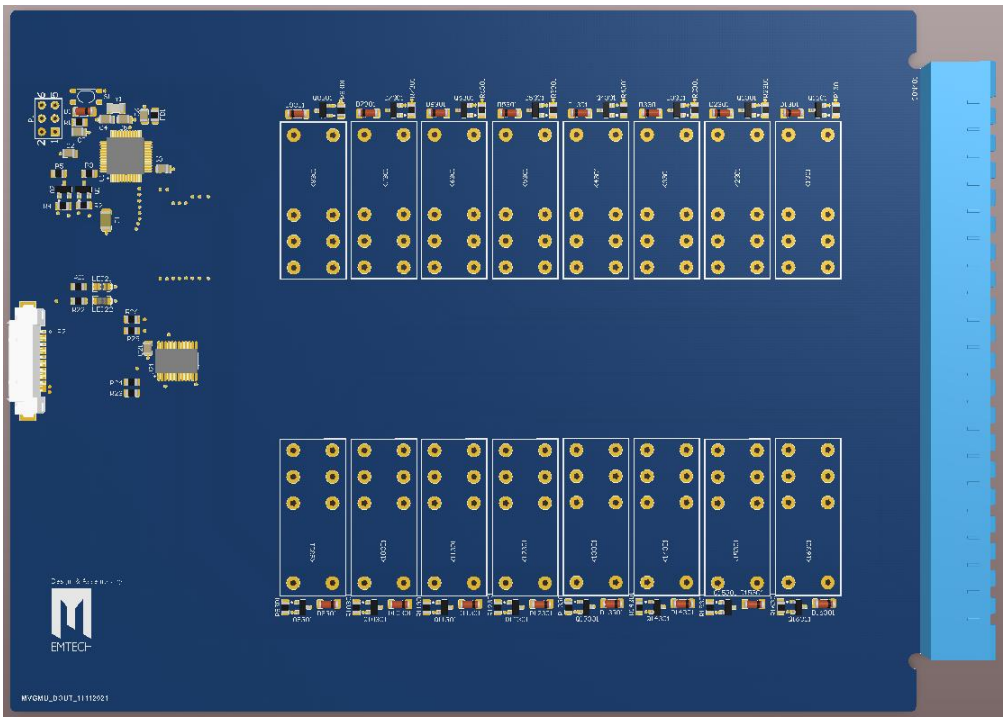

Figure 16: Digital output interface PCB

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3.1.3.3 Analogue Input

Figure 17 below shows the logical structure of the analogue input interface. As depicted, the interface consists mainly of an optocoupler to provide the isolation needed and to convert the input loop current to voltage, which is acquired by the MCU using an ADC. The Zener diode is used as a voltage regulator to power the circuitry of the left side (before the isolation). This is a typical isolated 4-20mA input commonly found in industrial environments where devices and equipment support such interfaces. Optocoupler's specifications:

- Low nonlinearity: 0.01%
- Insulation: 5 kV rms/1 min rating
- Low gain temperature coefficient: -65 ppm/°C
- Wide bandwidth – DC to >1 MHz

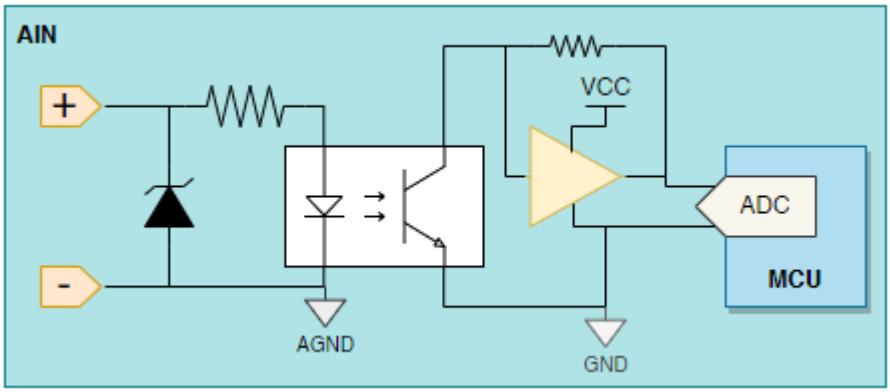

Figure 17: Analogue input logical structure

Figure 18 below depicts a 3D picture of the analogue input interface PCB showing its components placed on the board.

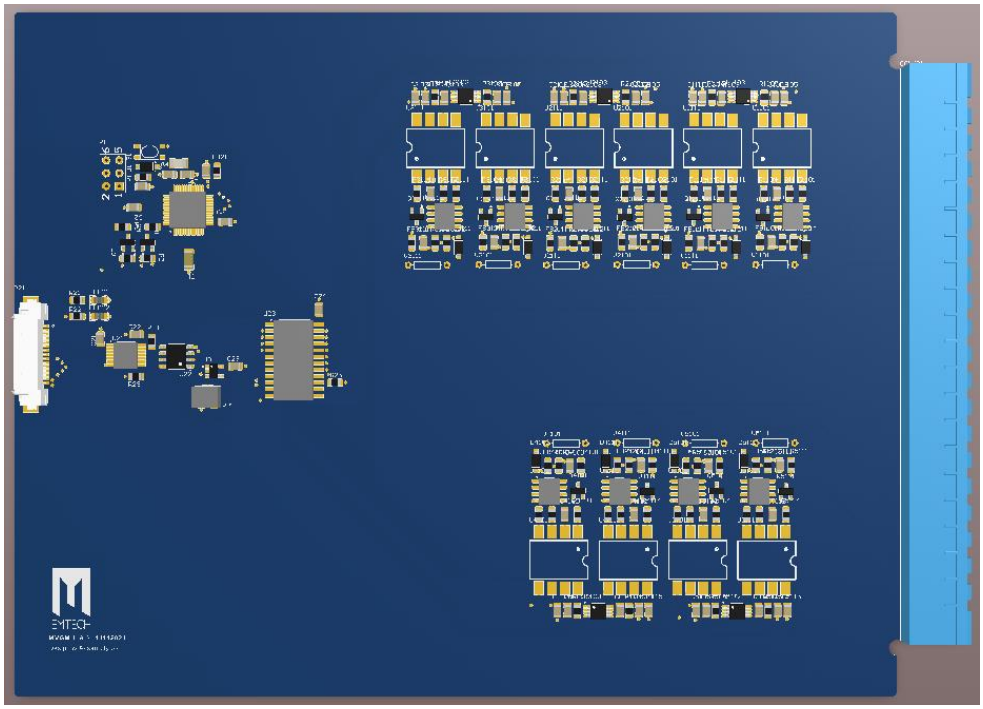

Figure 18: Analogue input PCB

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3.1.3.4 Analogue Output

Figure 19 below shows the logical structure of the analogue output interface. As depicted, it consists of a simple voltage to current converter using a digital potentiometer and amplifier, controlled by the MCU. In addition, an optocoupler is used to provide the isolation needed, and a DC/DC converter to power the circuitry of the interface and regulate the loop current according to the input configured from the MCU. The optocoupler is the same one used in the analogue input design. Figure 19 provides a simplified diagram of the analogue interface w.r.t. the electronic circuit with aim to show only its main elements. In addition, this is an active analogue output, therefore, no external power supply is required, as this is included, as stated above. The polarity of the output is designated as such to indicate that the terminals are connected to an analogue input in series, which means that the positive output terminal (AOUT+) is connected to the negative input terminal of an analogue input (AIN-) (Figure 17).

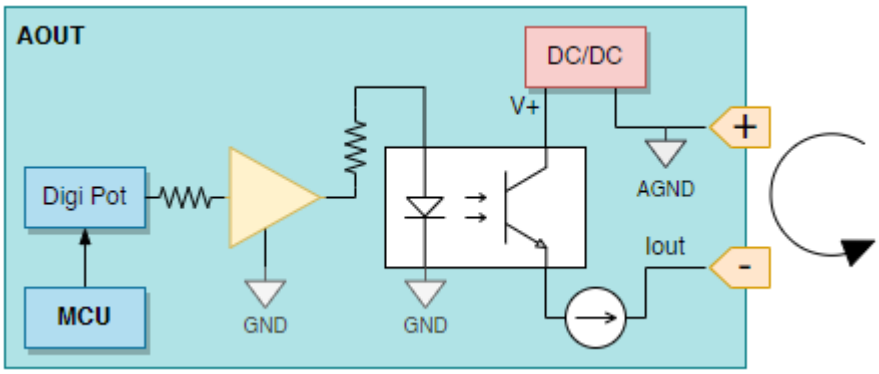

Figure 19: Analogue output logical structure

Figure 20 below depicts a 3D picture of the analogue interface PCB showing its components placed on the board.

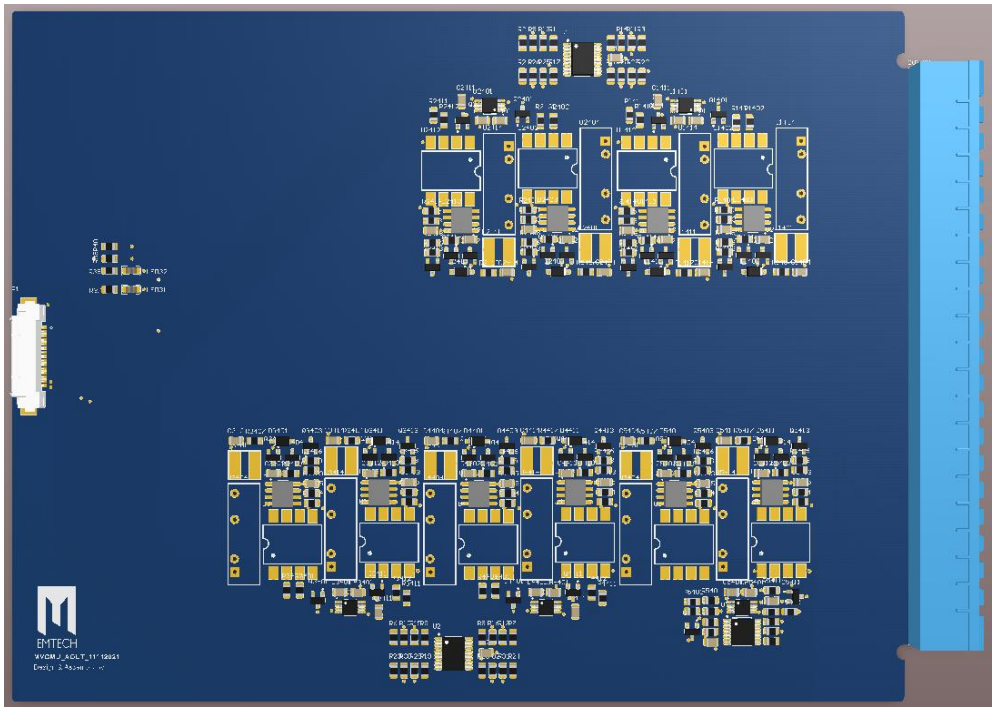

Figure 20: Analogue output interface PCB

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3.1.4 Phasor Measurement Unit

This section describes the Phasor Measurement Unit depicting its top-level structure and its interfaces with other modules. Main goal of the PMU is to measure the voltage and the current of the transformer, therefore, its logical structure include three key parts, as depicted in Figure 21 below:

1. Analogue front-end (AFE): for isolating the voltage input and reducing it to an acceptable level to acquire it, and for amplifying the current input from the current sensors. This consists of a total six (three for voltage and three for current) channels. The voltage input includes a differential isolation amplifier in combination with a voltage divider to reduce the input voltage and isolate it from the digital circuit. The current input includes a simple amplifier circuitry to amplify the input signal.
2. ADC: for digitizing the analogue input signal. This is a 6-channel high-speed simultaneous-sampling ADC with 16-bit resolution and fully differential bipolar inputs.
3. DSP: for handling the acquisition and communication. Essentially, this is the brain of the module running a firmware that handles all operations related to data acquisition, synchronization, communication and configuration. This is a high-performance low-power fixed-point Digital Signal Processor from Texas Instruments [RD-2], specifically:
   - Up to 200MHz clock rate
   - 13.33 to 5 ns Instruction Cycle Time
   - One or Two instructions executed per cycle
   - Dual Multiply-and-Accumulate Units
   - Two Arithmetic and Logic Units (ALUs)
   - Total of 320KB On-Chip RAM
   - 128KB On-Chip ROM
   - Tightly Coupled FFT Hardware Accelerator
   - Peripherals: McSPI, McBSP, UHPI, EMIF, UART, USB, DMA, eMMC, SPI, I2C, I2S

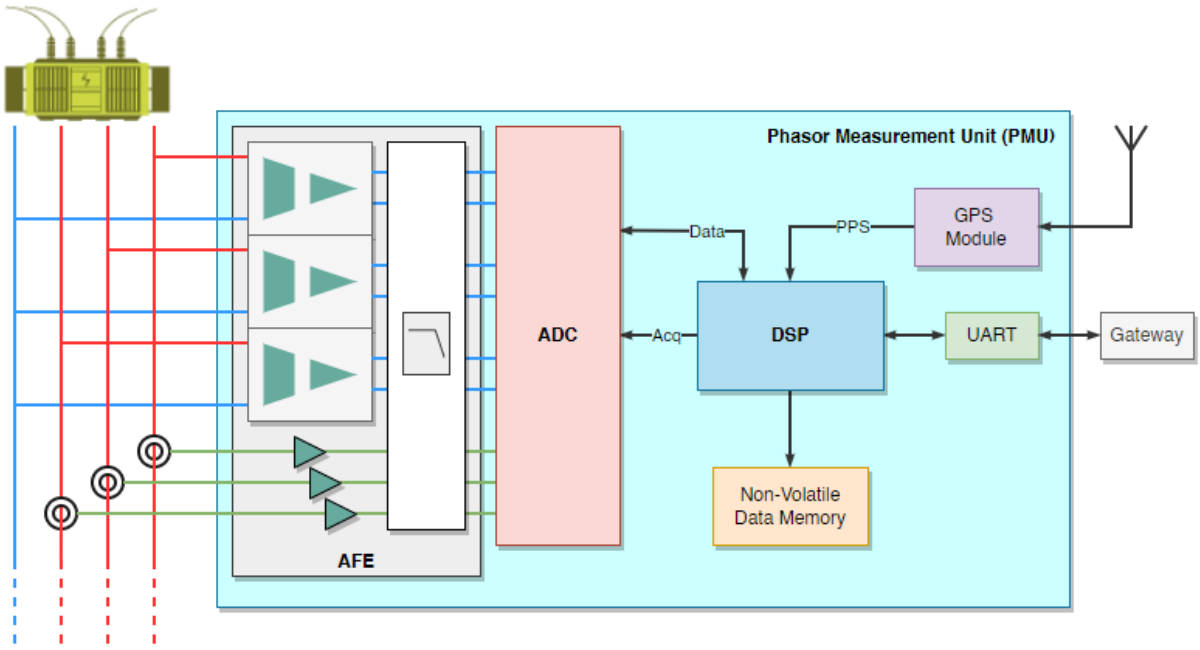

Figure 21: PMU logical structure

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Moreover, the module includes a non-volatile memory (SD card) for storing the acquired data and other parameters for configuring the device. The default storage size is 64GB, which is enough to store data for up to a year, but certain device parameters may be configured to adjust this time window, for example, the time interval between different data sets stored can be configured to have more data per time frame. A GPS module is included to acquire the time and the PPS signal for synchronizing the measurements between other MVGMU devices. A UART interface is utilized for communicating with the gateway module to configure the PMU module and to grab the acquired data for analysis according to certain features set by the grid resilience algorithms.

As aforementioned, the DSP is one of the key components in the PMU module. To simplify the overall design and the utilization of the DSP into different devices, a segregation was made regarding the DSP to have its own design. This way, a separate board is designed to include all the necessary components required for the DSP to operate with aim to keep the digital high-speed electronics section segregated and to expose all the necessary interfaces via a common board-to-board mezzanine connector. The idea is that the DSP board is mounted onto the main board of the PMU module, which has simpler design and uses only the necessary interfaces required. Figure 22 below shows the top side of DSP board depicting its main components (DSP, external memory modules, power regulator, crystal etc.) and Figure 23 shows the bottom side of the same board depicting the mezzanine connector where common DSP interfaces are exposed.

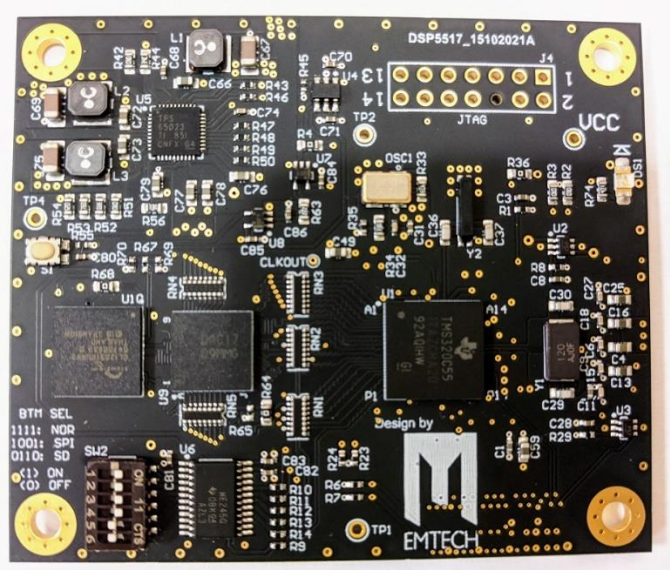

Figure 22: DSP board (top side)

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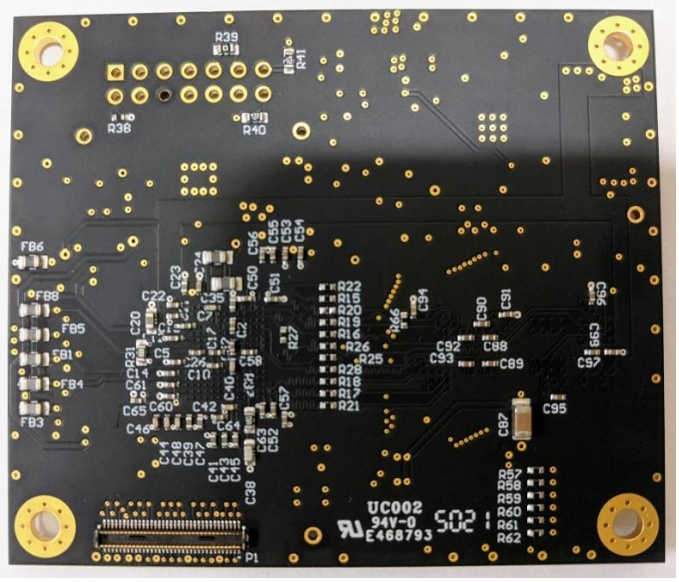

Figure 23: DSP board (bottom side)

The integration of the PMU module, and eventually of the LVGMU device, with the transformer is done directly. Specifically, the voltage inputs are directly connected to the low-voltage side of the transformer, three inputs correspond to the three grid phases. The current inputs, on the other hand, are connected using Rogowski coil sensors that measure the current through each phase line. The device is designed to accommodate different types of Rogowski coil sensors by simply configuring a specific parameter to translate the output of the sensor to units of Ampere.

3.1.5 Power Supply Unit

The power supply unit of the MVGMU device includes an input EMC filter and a DC/DC converter, as depicted in Figure 24 below. The MVGMU takes in power from primary substation's battery, which is 110VDC. The input EMC filter provides robustness and stability according to EMC engineering process, manufacturer recommendations, and EMC common practices. The DC/DC converter, from Traco Power [RD-4], is required to convert the input of 110VDC to provide the standard 5V power to the device

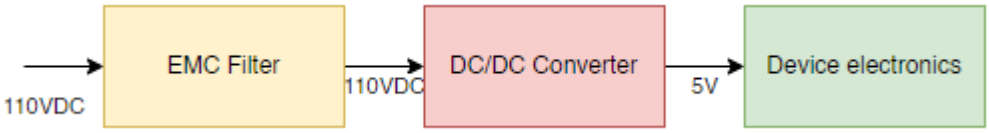

Figure 24: Power supply unit logical diagram

3.1.6 Mechanical Description

The MVGMU device is housed into a DIN 43700 panel-mount 144x288x179 mm enclosure. On the front side the display and the keypad are mounted, and on the rear side screw terminal type connectors are connected to interface with external elements. Figure 25 below shows a diagram that combines the logical elements of the MVGMU device with respect to its mechanical aspects, and as shown, a backplane includes mezzanine connectors to connect each individual vertical board that houses the corresponding module electronics. The backplane is a PCB placed near the front side

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of the enclosure, onto which the display, the keyboard, and the MCU are placed. The backplane board and the DIN, DOUT, AIN, AOUT boards comprise the DAQC module described in section 3.1.3 above. Figure 26 & Figure 27 below provide clearer picture regarding the inner arrangements of the PCBs inside the enclosure showing the front and the rear side respectively. Figure 28 & Figure 29 depict the front and the rear view of the enclosure showing the exterior of the device.

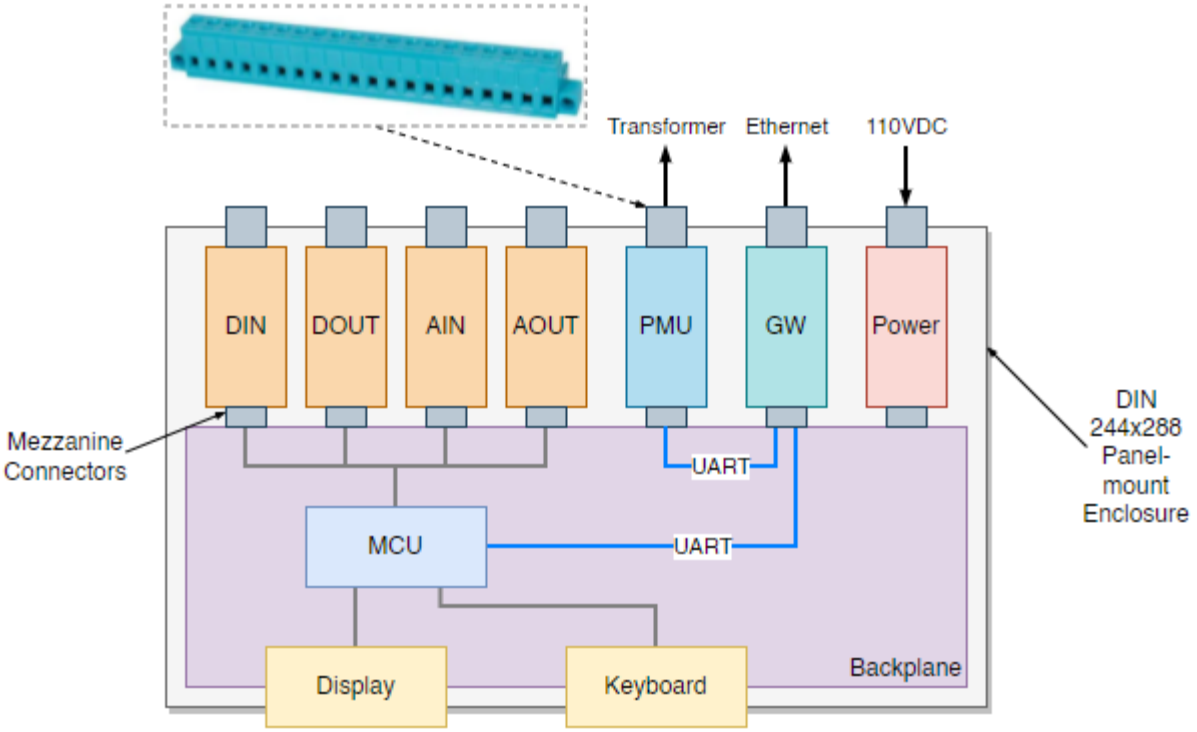

Figure 25: MVGMU mechanical information

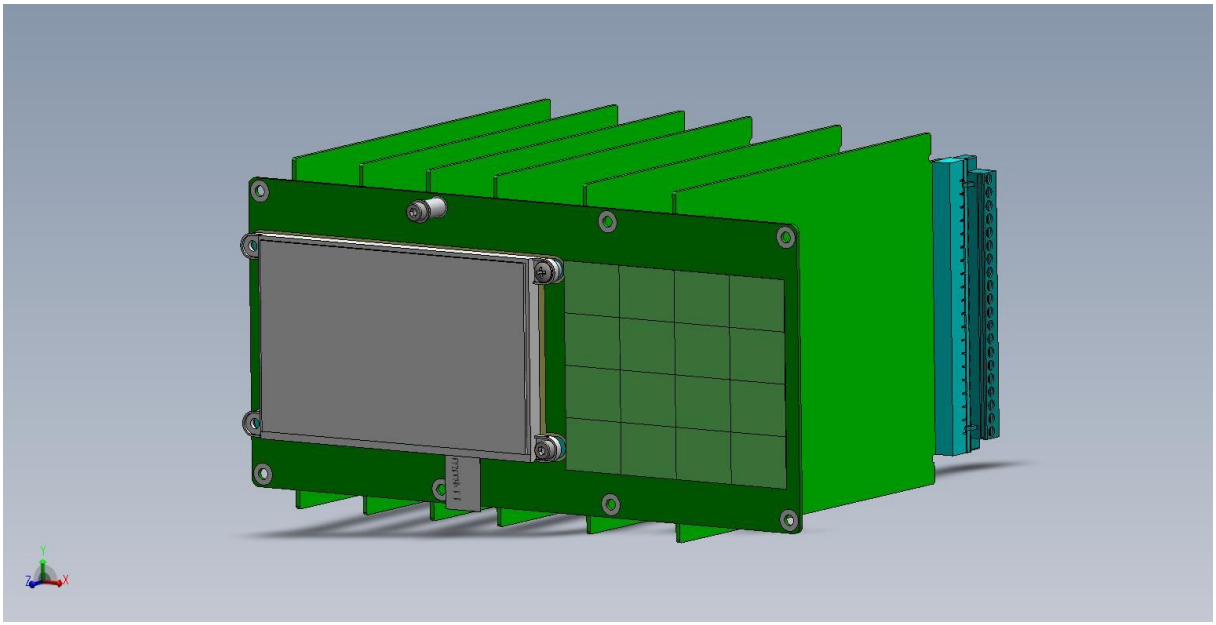

Figure 26: MVGMU inner enclosure view from the front

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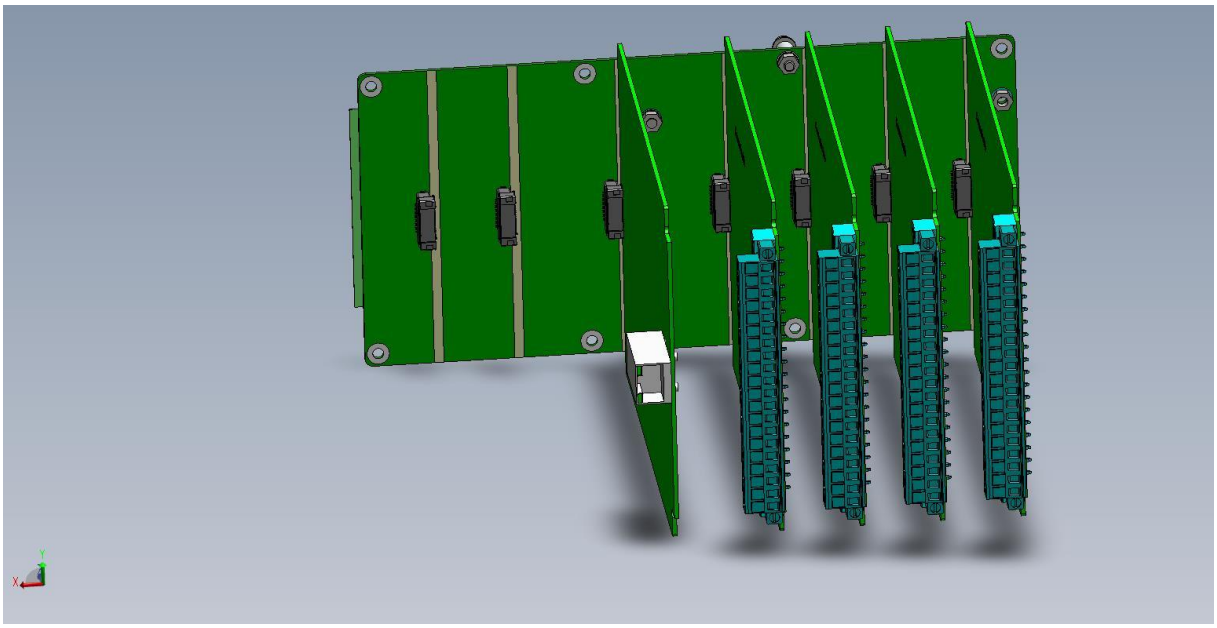

Figure 27: MVGMU inner enclosure view from the rear

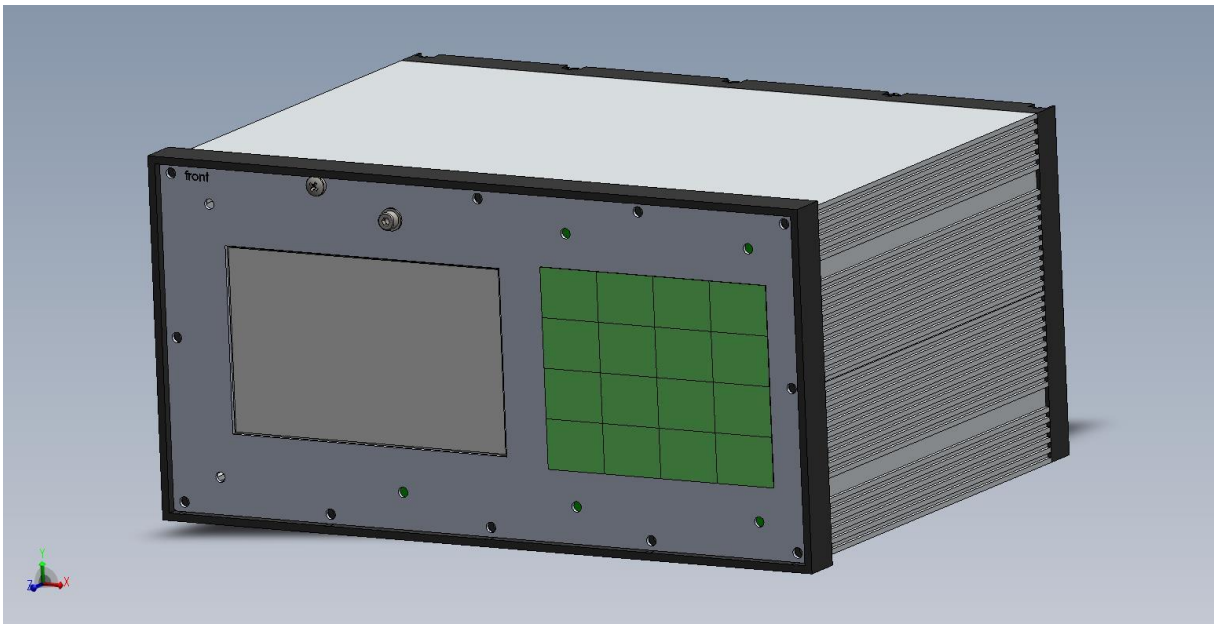

Figure 28: MVGMU enclosure front side

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Figure 29: MVGMU enclosure rear side

3.1.7 **Firmware**

This section describes the firmware of the MVGMU device. In general, the firmware (FW) is the low-level software that resides in the memory of a processor unit (a microcontroller or a DSP) and it contains the implementation required to make the device simply works in terms of operation, functionality, data handling, and I/O control. As aforementioned, the segregation of modules resulted to have two different firmware implementations, each residing in its own processing unit. Specifically, there is a firmware that resides in the MCU of the DAQC module, and another one that resides in the DSP of the PMU module. The following text provides a description regarding the structure of each FW, and as it is shown, this structure follows the same principle regarding architecture.

The FW of the PMU is divided into four main layers, drivers, support libraries, processes, and application, as show in Figure 30 below. The structuring of all four layers is based on the pattern where always higher-level layers utilize elements from lower-level layers. List below provides a description regarding each layer:

Driver: low-level driver implementation regarding certain internal DSP modules and external ICs. This layer provides basic functionalities to control low-level operations of the DSP and other peripherals including the following:

- McSPI
- I2C
- UART
- MMC
- EMIF
- DMA
- GPIO
- ISR
- ADC

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- NOR flash, and SDRAM memories

Support: API to be used by processes to access low-level functionalities. This includes the terminal prompt interface, the File System, and the XTERM support library, which is an implementation of the XMODEM protocol [RD-6] used in In-System-Programming (ISP) to support future FW updates.

Process: High and low priority processes related to device operation, including data acquisition (ACQ), data handling (DH), communication with the GW module (REMOTE), and the command prompt.

Application: top-level application related to the actual functional operation of the PMU module regarding measurement. Essentially, this is a single entity that combines different processes to accomplish a certain task.

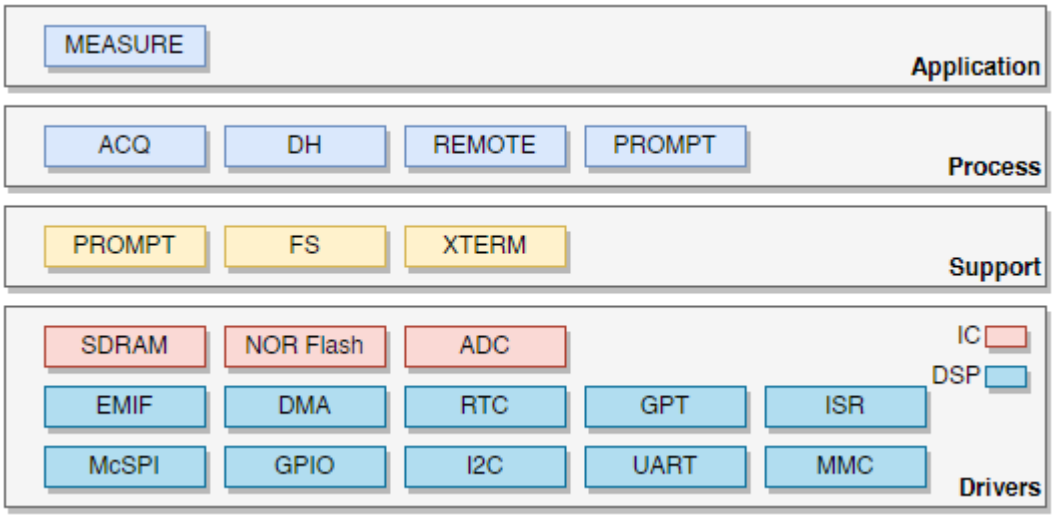

Figure 30: MVGMU – PMU Firmware structure

Similarly, the FW of the DAQC module follows, as mentioned above, the same design principle, which is based on organizing the various elements into layers. Figure 31 below shows its elements sorted into the four main layers. More specifically:

Driver: this includes low-level driver implementation regarding internal MCU modules and external ICs & components.

- SPI
- I2C
- UART
- GPIO
- GPT
- ISR
- ADC
- Display
- Keypad
- DigiPot
- RTC

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Support: This includes the terminal prompt interface, and the XTERM support library.

Process: This includes communication with the GW module (REMOTE), the command prompt interface, the user interface, and the I/O interfaces control.

Application: top-level application related to the actual functional operation of the DAQC module regarding measurement.

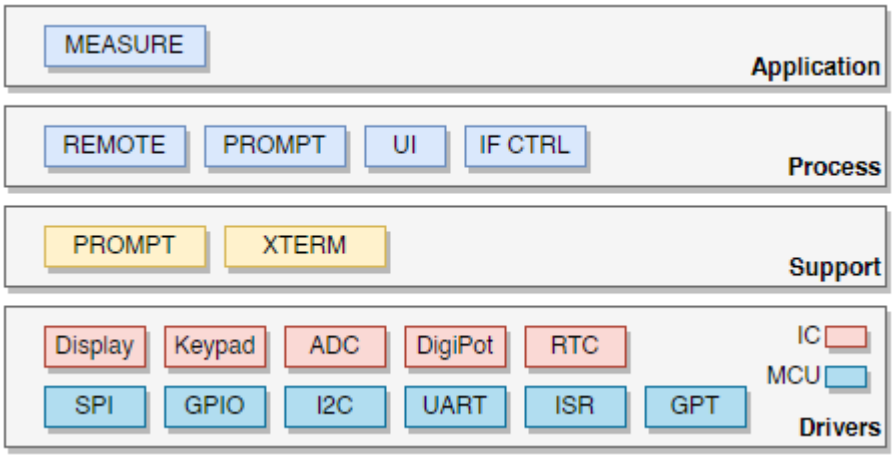

Figure 31: MVGMU – DAQC Firmware structure

3.1.8 Product Tree

Figure 32 below depicts the product tree of the MVGMU device illustrating the components that comprise it. Essentially, it is a block diagram that illustrates the incorporated constituents as entities w.r.t. the modules included, the hardware design files (schematics, PCB file, and BoM), the firmware or software running in the corresponding module, and the user manual. The number located in the bottom left corner of each SCH block indicates the number of schematic sheets that comprise that particular component.

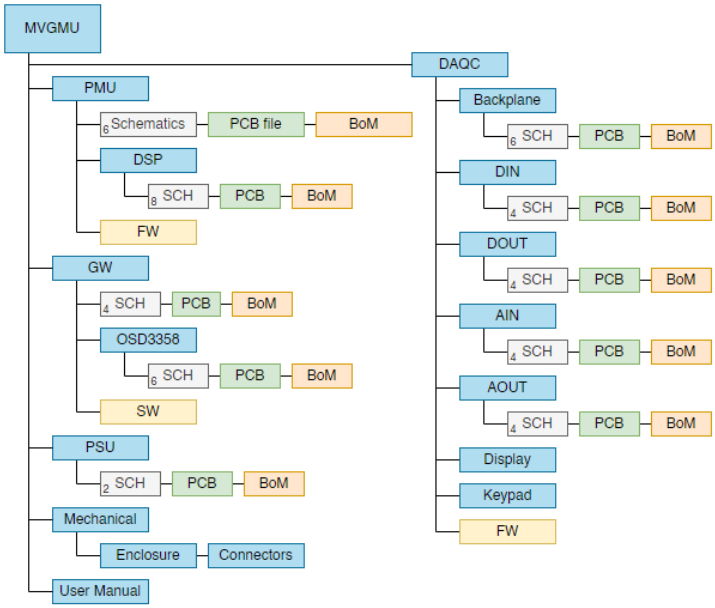

Figure 32: MVGMU product tree

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3.1.9 Specifications

This section provides a list of specifications regarding the MVGMU device related to key-features, functionalities, and interfaces.

Functionalities

- Primary substation automation unit
- Capacitor Bank Management
- OLTC management
- Transformer monitoring
- Phasor Measurement Unit
- Power quality measurements

Key-features

- High-end Processor running Linux OS
- EDGE computing capability
- Digital Signal Processor for high-rate sampling and fast processing
- Ethernet communication interface
- Isolated Analogue & Digital I/Os (4-20mA, relay)
- Voltage and current inputs

User Interface

- Display: 5.0” TFT colour LCD
- Keypad: 16-key membrane keypad

Communication Interface

- Ethernet: RJ-45
- Protocols: MODBUS TCP

Real-Time Clock

- Time: Hours, Minutes, Seconds
- Date: Day, Month, Year, Day name
- Battery retention: 10 years

Analogue Output

- Number: 10 per device
- Current Output Signal Range: 4-20mA
- Max Current Output: 23mA
- Non Load Voltage: 12V
- Output Power: 1Watt
- DA Conversion Frequency: 10 samples/sec
- Accuracy: 16-bit
- Error: 0.1 % Full Scale
- Linearity: < 0.01 % Full Scale
- Ripple: < 20mV (at 250 Ω)
- Isolation: Optical Isolation
- Configurable: Yes

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Analogue Inputs

- Number: 10 per device
- Input Signal Range: 4-20mA
- Load Impedance: approx. 135 Ω at 10mA, 270 Ω at 20mA
- Sampling Frequency max: 100 sample/sec
- Accuracy: 16-bit
- Error: 0.1 % Full Scale
- Linearity: < 0.01 % Full Scale
- Isolation: Optical Isolation
- Configurable: Yes

Digital Inputs

- Number: 10 per device
- Range: 23VDC – 140VDC
- Dielectric Insulation: 2.5kV peak at 50Hz
- Isolation: Optical Isolation

Digital Outputs

- Number: 10 per device
- Type: Relay Contacts
- Contact Rating: 250VAC / 8A
- Cycles: 50 000 – 100 000
- Insulation Coil-Contact: 3000 – 5000 Vrms
- Insulation Open Contact Circuit: 500 – 1000 Vrms

Voltage Inputs

- Number: 3, one per phase
- Input range: 230VAC nominal
- Isolation: optical isolation
- Isolation voltage: 4000Vpeak
- Transient Immunity: 10kV/us Minimum
- Sampling frequency: 10KHz
- Resolution: 16-bit

Current Inputs

- Number: 3, one per phase
- Type: Rogowski Coil sensor
- Range: 100mV/1000A typical, but configurable for different sensors
- Sampling frequency: 10KHz
- Resolution: 16-bit

Mechanical

- DIN 43700 panel-mount
- Dimensions: 144x288x179

Power Input

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- Input range: 36-160 VDC, 110 VDC nominal
- Isolation: 4000VAC
- Consumption: 25 Watt max

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3.2 LVGMU

3.2.1 Gateway

Refer to section 3.1.1 for the description of the GW module. Its structure in the LVGMU device is the same and it's based on the same design used in the MVGMU device.

3.2.2 User Interface

No User Interface is utilized in the LVGMU device.

3.2.3 Data Acquisition and Control

No DAQC module is utilized in the LVGMU device.

3.2.4 Phasor Measurement Unit

Refer to section 3.1.4 for the description of the PMU. The same logical design is used in the LVGMU device, same components and same parts.

3.2.5 Power Supply Unit

The power supply unit of the LVGMU is kept simple and it consists of mainly two parts, the AC power entry line filter and the AC/DC converter. The LVGMU device takes in power from a 230VAC source. Two options are considered regarding the mechanical aspects of the power entry depending on the source, however, only one option is supported at a time, so it must be decided before hand which is the most suited option for the application, mainly taken into account the installation site environment. More specifically, if the device is intended to be powered from a wall socket then an IEC C14 panel mount plug is fitted. This is part of the line filter module as shown in Figure 33 below, which is a panel mount AC power entry module that includes the line filter, a fuse holder, and IEC C14 plug enclosed into a single module. The second option is to power the LVGMU device directly from the transformer by connecting the power input internally to one of the phases, phase 1 by default. This way, a different power entry filter module is used, shown in Figure 34, which is a chassis mount type module. Independent of what option is provided, the filtered 230VAC line is fed into the AC/DC converter to provide the 5V power to the electronic board of the device. The AC/DC converter is a 5 Watt encapsulated in a compact plastic case, as shown in Figure 35, suitable for industrial applications.

Figure 33: LVGMU power line filter (Option 1)

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Figure 34: LVGMU power line filter (Option 2)

Figure 35: LVGMU AC/DC converter

3.2.6 **Mechanical Description**

The LVGMU is housed in a Polycarbonate enclosure of size 300x200x90 mm. Figure 36 below shows the connections between the LVGMU and the external elements, the types of cables used, and information about the connectors used. As depicted, the cable used to connect to the transformer is a 4x2.5mm2 cable, but other types with thinner inner wires can also be used, though, the size of the cordgrip used (M20) can accept cables of 12mm maximum diameter. Same type cordgrips, but smaller size (M12), are used to hold the Rogowski coil sensor cables entering the enclosure. For the power input an IEC C14 plug is used, which is part of the input main's filter that is included. For the network interface a common panel-mount RJ45 connector is used to provide the Ethernet interface required. Finally, an SMA connector is provided for the connection of the GPS antenna. The LVGMU device does not include any switch, the second it is plugged into the power it starts operating.

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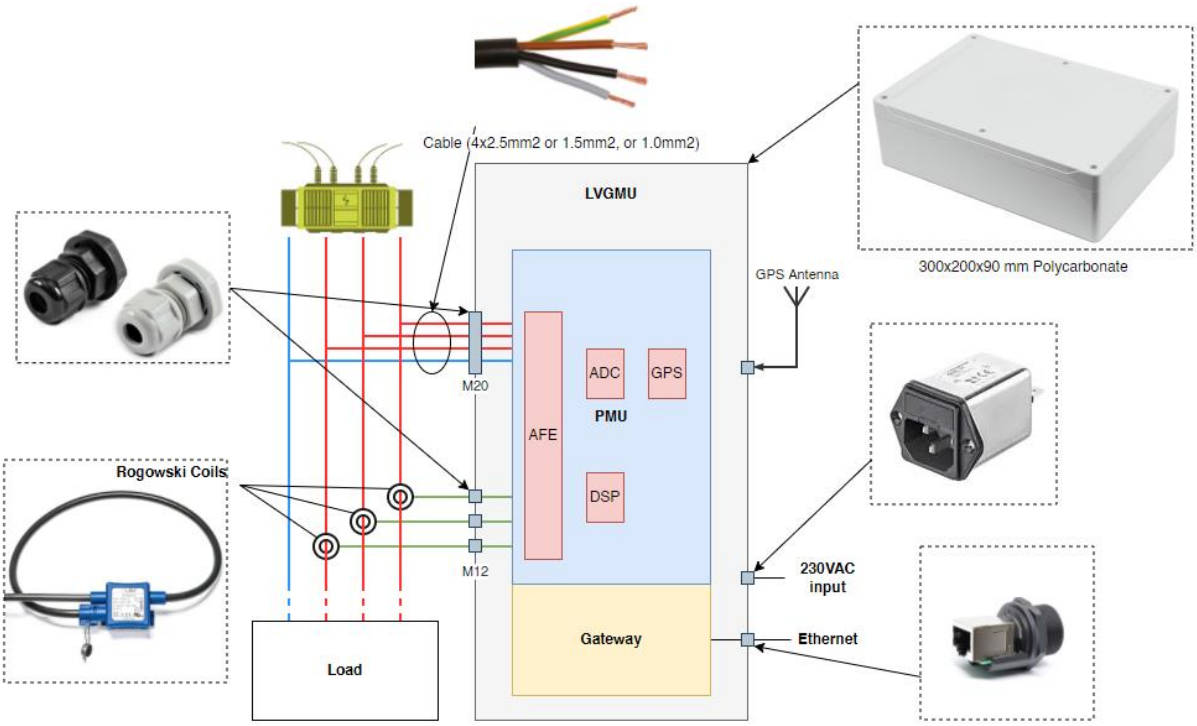

Figure 36: LVGMU mechanical information

Figure 37 below shows the PCB of the LVGMU device. Inner sections are highlighted, specifically, the AC/DC converter, the GPS, the Gateway, the DSP, and the AFE, as well as the interfaces, the 230VAC power input, the voltage & current inputs, and the Ethernet interface.

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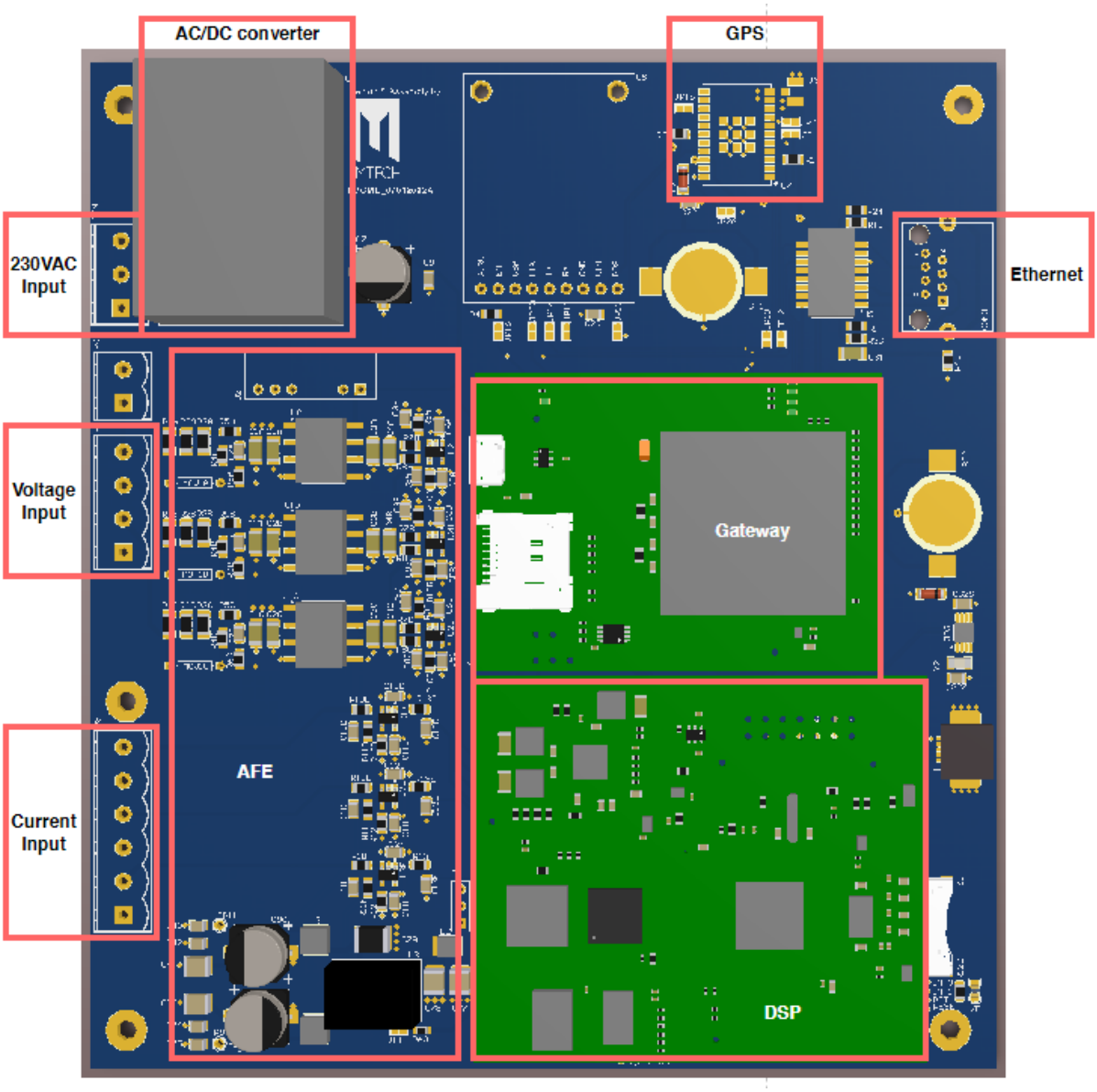

Figure 37: LVGMU PCB

3.2.7 Firmware

Refer to section 3.1.7 above for the description of the PMU firmware.

3.2.8 Product Tree

Figure 38 shows the product tree of the LVGMU device illustrating the components that comprise it.

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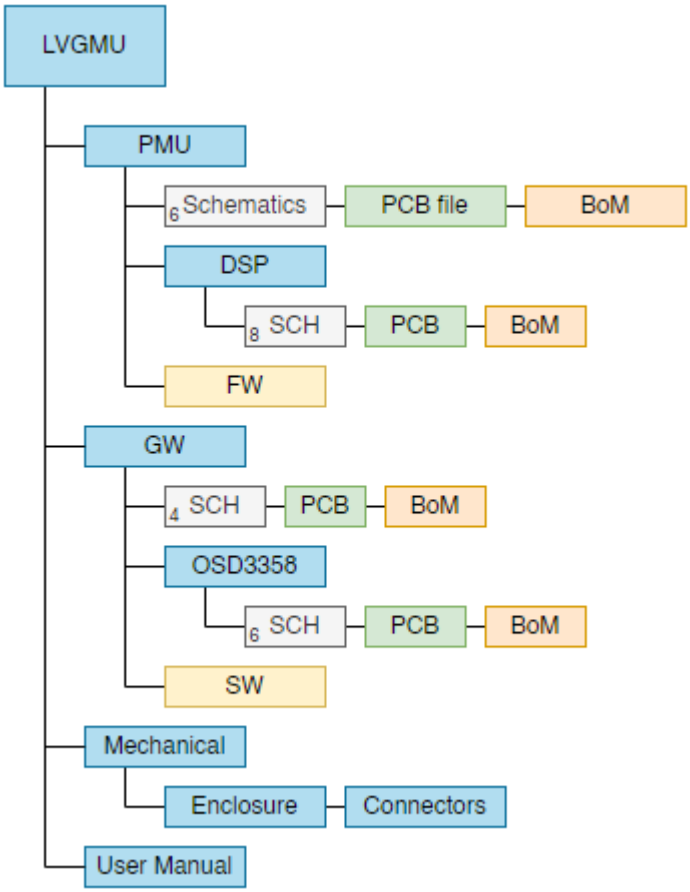

Figure 38: LVGMU product tree

3.2.9 Specifications

This section provides a list of specifications regarding the LVGMU device related to key-features, functionalities, and interfaces.

Functionalities

- Secondary substation automation unit
- Transformer monitoring
- Phasor Measurement Unit
- Power quality measurements

Key-features

- High-end Processor running Linux OS
- EDGE computing capability
- Digital Signal Processor for high-rate sampling and fast processing
- Ethernet communication interface
- Voltage and current inputs

Communication Interface

- Ethernet: RJ-45
- Protocols: MODBUS TCP

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Real-Time Clock

- Time: Hours, Minutes, Seconds
- Date: Day, Month, Year, Day name
- Battery retention: 10 years

Voltage Inputs

- Number: 3, one per phase
- Input range: 230VAC nominal
- Isolation: optical isolation
- Isolation voltage: 4000Vpeak
- Transient Immunity: 10kV/us Minimum
- Sampling frequency: 10KHz
- Resolution: 16-bit

Current Inputs

- Number: 3, one per phase
- Type: Rogowski Coil sensor
- Range: 100mV/1000A typical, but configurable for different sensors
- Sampling frequency: 10KHz
- Resolution: 16-bit

Mechanical

- Material: Polycarbonate enclosure
- Dimensions: 300x200x90 mm
- Protection: IP68
- Liquid-Tight Cordgrips for cable I/O

Power Input

- Input range: 90-305VAC
- Isolation: 4000VAC
- Consumption: 5 Watt max
- Other: option to power from phase A and neutral

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3.3 DERMU

3.3.1 Gateway

Refer to section 3.1.1 for the description of the GW module.

3.3.2 User Interface

The User interface in the DERMU is kept simple, only two Buttons and four LEDs are provided to the end-user as input to the device to execute a specific function and respectively as output to provide an indication regarding certain operation or behaviour.

3.3.3 Data Acquisition and Control

Refer to section 3.1.3 for the description of the DAQC module. From a logical perspective this module remains the same, however, considering that this is a different device, housed in a different enclosure, the number of channels of each interface is reduced to two and the electronics that comprise them are placed onto a single PCB.

3.3.4 Power Supply Unit

The power supply unit of the DERMU device includes an input EMC filter and a DC/DC converter, as depicted in Figure 39 below. The DERMU takes in power from an external 24VDC power supply to comply with common industrial operation standards. The input EMC filter provides robustness and stability according to EMC engineering process, manufacturer recommendations, and EMC common practices.

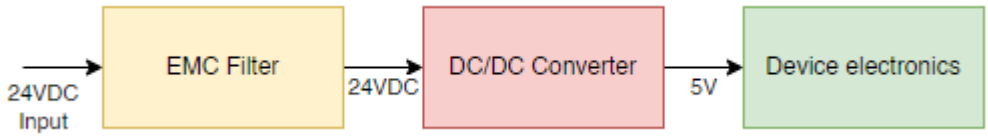

Figure 39: DERMU power supply unit logical diagram

Figure 40 below depicts the power supply unit of the DERMU device showing its components, the input connector, the switch, the fuser holder, the EMC filter, and the DC/DC converter.

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Figure 40: DERMU power supply unit

3.3.5 **Mechanical Description**

The DERMU device is housed into a DIN rail EN60715 mountable enclosure made of a combination of aluminium and polystyrene material. It has IP50 class protection, its size is 210x105x75 mm, and it weighs less than 1Kgr. The connectors are vertical screw terminal connectors. Figure 41 below shows a picture of the enclosure.

Figure 41: DERMU enclosure

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Figure 42 below shows a 3D representation of the DERMU PCB highlighting its main interfaces and components. On the top side, from left to right, the user interface is shown, the analogue inputs, the analogue outputs, the 24VDC power input, the fuse holder and the power switch. On the bottom side, the Ethernet connector is show, the RS-485 interface, the RS-232 interface, the digital output, and the digital input interface. The green board labelled “Gateway” is the OSD3358 board, part of the gateway module.

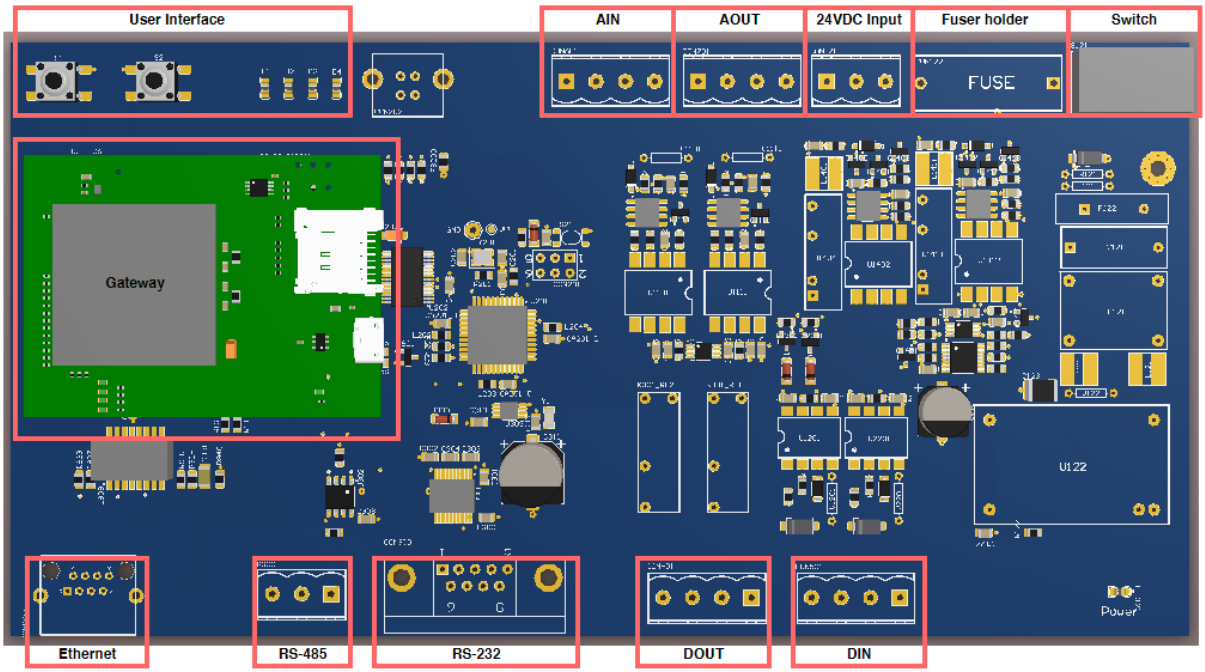

Figure 42: DERMU PCB

3.3.6 **Firmware**

Refer to section 3.1.7 above for the description of the DAQC firmware.

3.3.7 **Product Tree**

Figure 43 shows the product tree of the DERMU device illustrating the components that comprise it.

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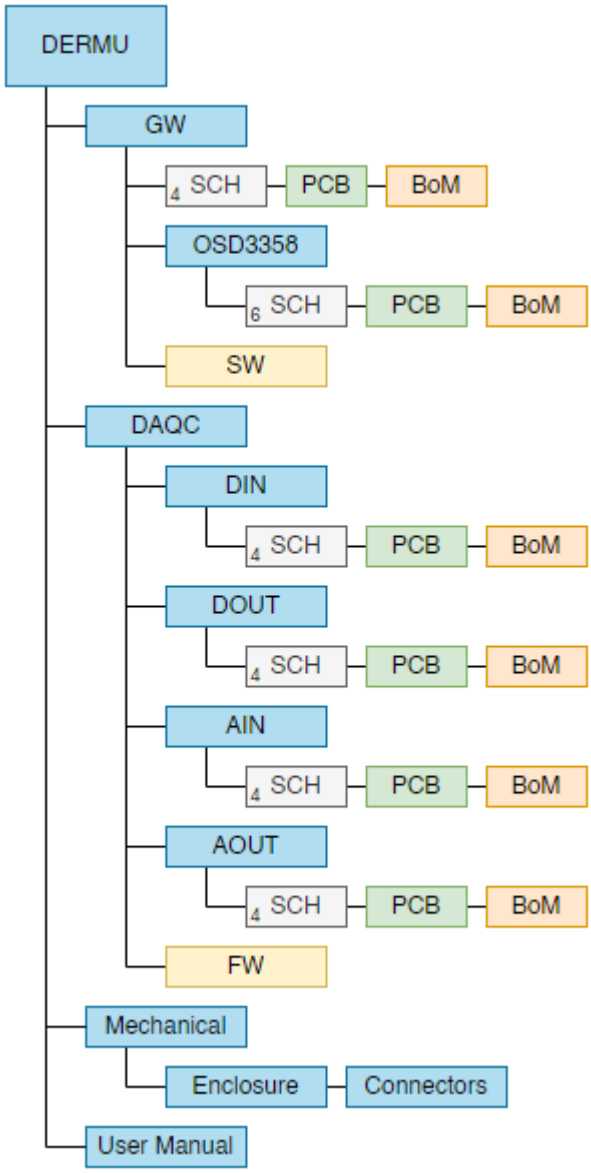

Figure 43: DERMU product tree

3.3.8 Specifications

This section provides a list of specifications regarding the DERMU device related to key-features, functionalities, and interfaces.

Functionalities

- DER assets monitoring and control
- Grid management at DER sites

Key-features

- High-end Processor running Linux OS
- EDGE computing capability
- Ethernet communication interface
- Isolated Analogue & Digital I/Os (4-20mA, relay)

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User Interface

- Input buttons
- LEDs indicators

Communication Interface

- Ethernet: RJ-45
- Protocols: MODBUS TCP

Real-Time Clock

- Time: Hours, Minutes, Seconds
- Date: Day, Month, Year, Day name
- Battery retention: 10 years

Analogue Output

- Number: 2 per device
- Current Output Signal Range: 4-20mA
- Max Current Output: 23mA
- Non Load Voltage: 12V
- Output Power: 1Watt
- DA Conversion Frequency: 10 samples/sec
- Accuracy: 16-bit
- Error: 0.1 % Full Scale
- Linearity: < 0.01 % Full Scale
- Ripple: < 20mV (at 250Ω)
- Isolation: Optical Isolation
- Configurable: Yes

Analogue Inputs

- Number: 2 per device
- Input Signal Range: 4-20mA
- Load Impedance: approx. 135Ω at 10mA, 270Ω at 20mA
- Sampling Frequency max: 100 sample/sec
- Accuracy: 16-bit
- Error: 0.1 % Full Scale
- Linearity: < 0.01 % Full Scale
- Isolation: Optical Isolation
- Configurable: Yes

Digital Inputs

- Number: 2 per device
- Range: 23VDC – 140VDC
- Dielectric Insulation: 2.5kV peak at 50Hz
- Isolation: Optical Isolation

Digital Outputs

- Number: 2 per device
- Type: Relay Contacts

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- Contact Rating: 24VAC / 3A

Mechanical

- Mounting: DIN Rail EN 60715
- Material: Polystyrene/Aluminium
- Protection: IP50
- Dimensions: 210x105x75 mm

Power Input

- Input range: 9-40VDC, 24VDC nominal
- Isolation: 3000VACrms
- Consumption: 3 Watt max

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4 Conclusion

Grid resilience at LV/MV heavily relies on the monitoring, automation and control of key assets like the primary, secondary substations and the distributed energy resources with significant impact across the distribution lines. This is achieved by utilizing the grid management units MVGMU, LVGMU and DERMU as described in detail in this document. However, having a set of automation units does not complete the whole puzzle of achieving the appropriate flexibility of energy grids and increase their resilience, a platform that combines hardware & software elements operating together is required to balance out the equation that optimizes the power grid and all the deployed assets with aim to maximize energy efficiency.

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